DRIVING METHOD OF SPEAKER AND THE DRIVING CIRCUIT THEREOF

BACKGROUND OF THE INVENTION

A. Technical Field of the Invention

The present invention relates to a driving method of speaker, and in particular, to a driving method and a driving circuit of speaker by the application of both pulse width modulation (PWM) and digital to analog converter (DAC) technique.

B. Description of the Prior Art

Digital sound playing is an important function of consumer electronic products. Generally, there are two basic types of driving method of outputting digital sound via speaker, i.e., digital to analog converter driving method and pulse width modulation driving method.

FIG. 1 illustrates a circuit diagram of traditional DAC. In this driving method, digital sound data are converted into analog signals with responding current value, and then these analog signals are directly drive the speaker. As shown in FIG. 1, each bit of digital sound data, Bit 0 ~ Bit 7, is used to control a corresponding current amplifier with different current ratio, and the output of each current amplifier are commonly connected to the speaker. During playing, digital sound data are sequentially input to the DAC with the speed of sampling rate. In integrated circuit design, each current amplifier and control switch can be implemented by MOS elements with different area.

FIGS. 2 and 3 illustrate the waveform modulated by PWM and its implementation structure. The action principle of PWM is to modulate sound amplitude onto pulse width, not onto pulse height. When the modulation pulse frequency is far higher than the sound frequency, the sound amplitude can be represented by pulse width and drive a speaker. Assume the PWM is implemented digitally and the amplitude, pulse width are equally divided into 255 parts, i.e. represented as 2^8, then the sound amplitude is 255 level, and pulse width is also represented by 255 level in the PWM. The waveform modulated by PWM is shown in FIG. 2 and its block diagrams are shown in FIG. 3. The action principle is that digital sound

data Wd and the output of a counter are input to a comparator at the same time. At the beginning of every sampling pulse, digital sound data Wd is input to the comparator and the counter starts to count. At this instance, the output of the comparator is HI. When the count value reaches the value of Wd, the output of the comparator is become LOW. Thus, the waveform of FIG. 2 is obtained.

Under this principle of PWM, the sound amplitude is represented by pulse width, and the pulse width is determined by the counting of a counter. Thus, the linearity of the sound driving signals are determined by the counter, and the clock pulse of the counter is provided by the quartz oscillator. Because the accuracy of quartz oscillator is high, thus, the advantage of PWM is that the linearity of the sound driving signals is good and the quality of sound can be easily controlled. In addition, the factors determining the sound quality for this sound driving method are as follows.

1) Modulation frequency; and

2) Sound resolution.

If the modulation frequency is too low, aliasing phenomenon will affect the sound quality. Thus, in the application of PWM, the modulation frequency has to be fixed. If the reference clock pulse in PWM is 4MHz, the acceptable lowest modulation frequency is assumed to be F Hz, then the sound level is 4M/F (integer). If the reference clock pulse in PWM becomes to 2MHz, then the sound level is lowered to 2M/F, which lowers the sound resolution, and the sound quality becomes poor. Thus, in the application of PWM, in order to achieve a specific sound quality, one basic requirement is the higher speed clock pulse.

However, the advantage of the DAC driving method is that the required clock pulse is equal to the sampling rate of sound signals, thus, the requirement of clock pulse is low. But the drawback is that the linearity of the amplifier is lowered while the required playing sound is large and the output current of each current amplifier is large. Thus, loss of fidelity of sound is occurred. In the PWM driving method, because sound amplitude is represented by

pulse width and the pulse width is determined by the counting of the counter, the linearity of sound is determined by the counter. As the linearity of the sound is determined by the counter, and the clock pulse of the counter is provided by the quartz oscillator with great accuracy, the linearity of the sound driving signals are good and the quality of sound can be easily controlled. The only drawback is that a higher speed clock pulse is required.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a driving method of speaker and the driving circuit thereof, wherein the driving signals are obtained by both PWM driving method and DAC driving method. It has the advantage of good linearity and the characteristics of low clock pulse in combination with DAC in improving the PWM at higher speed pulse. In accordance with the present invention, the method comprises the following steps.

1) dividing each digital sound data into two groups, i.e., higher bits data group and lower bits data group;

2) modulating one data group into driving signals represented by pulse width, i.e. this data group is modulated by PWM principle; and

3) converting the other data group into driving signals represented by pulse height, i.e., this data group is converted by DAC principle.

As a portion of digital sound data is converted by DAC, the clock pulse frequency required by PWM will be lowered accordingly, but the resolution of sound can be still maintained.

These and other aspects of the invention will be apparent from the elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of a conventional DAC driving structure.

FIG. 2 is a waveform modulated by a conventional PWM driving structure.

FIG. 3 is a circuit diagram of a conventional PWM driving structure.

FIG. 4 is a driving waveform modulated by the driving method of speaker of the present invention.

FIG. 5 is another driving waveform modulated by the driving method of speaker of the present invention.

FIG. 6 is a circuit diagram of the driving method of speaker of the present invention.

FIG. 7 is another circuit diagram of the driving method of speaker of the present invention.

FIG. 8 is a waveform by driving a sound signal in accordance with the driving method of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In accordance with the present invention, the driving method of speaker is first to divide digital sound data into two groups, i.e., higher bits data group and lower bits data group. One data group is converted by DAC method, and the other data group is modulated by PWM method so as to obtain the advantages of the low pulse frequency of DAC method and the good linearity of PWM method. There is no restriction to the implementation method of higher bits data either by DAC method or by PWM method.

In order to further understand the present invention, assume the digital sound data is 8 bits. The 8 bits data are divided into a data group with P bits data and the other group with D bits data. In this embodiment, the P is defined as 5 and regarded as pulse width resolution data and the D is defined as 3 and regarded as pulse heigh resolution data. FIGS. 4 and 5 show the waveform obtained by present invention for the digital sound data "11101101", wherein the P bits data group is higher bits data in FIG. 4, and P bits data group is lower bits data in FIG. 5.

Next, referring to FIG. 6, there is shown the first embodiment circuit structure of the driving method of the present invention. As shown in this drawing, the circuit comprises

PWM modulation circuit 10, DAC convert circuit 20, and speaker 30. The PWM modulation circuit 10 modulates P bits data into driving signals represented by pulse width, and DAC convert circuit 20 converts D bits data into driving signals represented by pulse height.

The PWM modulation circuit 10 comprises a counter 11, an accumulator 12, a first and second comparator 13, 14 and a XOR gate 15. The accumulator 12 receives the P bits data and adds 1 as its output. The first comparator 13 compares the counting value of the counter 11 with the output value of the accumulator 12 and outputs HI if the output value of the accumulator 12 is smaller than the counting value of the counter 11. The second comparator 14 compares the counting value of the counter 11 with the P bits data and outputs HI if the P bits data is smaller than the counting value of the counter 11. The XOR gate 15 receives the output of the first comparator 13 and the second comparator 14. In FIG. 6, Wd1 is the output value of accumulator 12 and Wd2 is the value of P bits data, B7~B3.

The DAC convert circuit 20 comprises three AND gates 21, 22, 23 and four current sources 24, 25, 26 and 27. One of the input terminal of each AND gate 21, 22, 23 connects to the D bits data, respectively, and the other input terminal is commonly connected to the output of the XOR gate 15. The four current sources 24, 25, 26, 27 have different current ratio, for example 8, 4, 2 and 1, and are controlled by the output of the second comparator 14 and the three AND gates 21, 22, 23, respectively. The output of each current source 24, 25, 26 and 27 are commonly connected to the speaker 30.

As shown in FIG. 4, the pulse width is $32(2^5)$ level, and the pulse height is $8(2^3)$ level. At the beginning of sampling pulse, P bits data, B7-B3 are input to the second comparator 14 and the accumulator 12. When Wd1, Wd2 are smaller than the counting value of the counter 11, the output of the first comparator 13 and the second comparator 14 is HI. When Wd1, Wd2 are greater or equal to the counting value of the counter 11, the output of the first comparator 13 and the second comparator 14 is LOW. Referring to FIG. 6, there is shown the

circuit structure. The action of the circuit is divided into three stages.

The first stage is that Wd1 and Wd2 is smaller than the counting value of the counter 11. At this stage, the output of the first and the second comparator 13, 14 are HI. Thus, the output of XOR gate is LOW. At this instance, the output of the three AND gates 21, 22, 23 connected to the XOR gate 15 is LOW, thus, the current sources 25, 26, 27 are OFF, but the current source 24 connected to the second comparator 14 is ON. Thus the pulse height of the driving signal at this stage is at level 8 and the pulse width is equal to Wd2 reference clock, illustrated by the first section of the waveform of FIG. 4.

The second stage is that Wd2 is equal to the counting value of the counter 11, but Wd1 is smaller than the counting value of the counter 11. At this stage, the output of the second comparator 14 is LOW, but the output of the first comparator 13 is HI, thus the output of XOR gate 15 is HI. At this instance, the current source 24 connected to the second comparator 14 is OFF, but the outputs of the other three AND gates 21, 22, 23 are dependent on the D bits data, B2-B0. As D bits data B2-B0 is "101", the output of AND gates 21, 23 is HI, and output of the AND gate 22 is LOW. Thus, the pulse height of the driving signals at this stage is at level 5 and the pulse width is equal to one reference clock, illustrated by the second portion of the waveform of FIG. 4.

The third stage is that Wd1 and Wd2 are greater than or equal to the counting value of the counter 11. At this stage, because the output of the first and the second comparator 13, 14 are LOW, the output of XOR gate 15 is LOW. Thus, the output of the three AND gates 21, 22, 23 connected to the XOR gate 15 are also LOW. At this instance, the four current sources 24, 25, 26, 27 are OFF. Thus, the pulse height of the driving signals at this stage is at level 0, illustrated by the third portion of the waveform of FIG. 4.

As shown in FIG. 6, the circuit structure employs five higher bits data as PWM control, thus, the waveform of the driving signals has a waveform alike the conventional PWM waveform. However, the different is that three lower bits data are converted into driving

signals by DAC with one reference clock width, such that the pulse level of PWM is lowered and the reference clock frequency is also lowered at the same time.

Next, referring to FIG. 7, there is shown the other embodiment of circuit structure of the driving method of the present invention. The circuit structure employs three higher bits data (B7-B5) as the D bits data to proceed with pulse height conversion, and employs other five lower bits data (B4-B0) as P bits data to proceed with pulse width modulation. As shown in this drawing, the circuit structure comprises PWM modulation circuit 10', DAC convert circuit 20' and speaker 30.

The PWM modulation circuit 10' is similar to the conventional PWM modulation circuit, comprises a counter 11' and a comparator 13' connected to the output of the counter 11' and the P bits data.

The DAC modulation circuit 20' comprises an accumulator 22' and a multiplexer 23'. The accumulator 22' receives D bits data and adds 1 as the output and the output of the accumulator 22' is 4 bits, D+1. The multiplexer 23' is a 2 to 1, 4-bits multiplexer. The multiplexer 23' receives the output of the accumulator 22' and the D bits data S2 as two inputs I1, I2 and receives the output of the comparator 13 as selection signal SEL. Because S2 is a 3-bits data, the highest bit of the input terminal I2 of the multiplexer 23' must be directly connected to the ground. In addition, the output of the multiplexer 23' respectively controls 4 current sources 24, 25, 26 and 27 with different current ratio. The output of these current sources 24, 25, 26, 27 are commonly connected to the speaker 30.

Next, referring to FIG. 7, describe the action of the circuit structure in accordance with the present invention. The action is divided into two stages.

The first stage is that the value of P bits data (B4-B0) is smaller than the counting value of the counter 11'. At this stage, the output of the comparator 13' is LOW. Thus, the multiplexer 23' selects the S1 as the output. As the data of S1 is greater than D bits data with 1, it indicates that the pulse height of driving signal is higher than the D bits data by one level.

And the pulse width of driving signal is the width represented by P bits data, illustrated by the first section of the waveform of FIG. 5.

The second stage is that the value of P bits data (B4-B0) is greater than or equal to the counting value of the counter 11'. At this stage, the output of the comparator 13' is HI, thus the multiplexer 23' selects the S2 as the output. At this instance, the pulse height of driving signal is equal to the value of D bits data and maintains to the end of this cycle, illustrated by the second portion of FIG. 5.

As shown in FIG. 7, the circuit structure employs higher bits data as the DAC control. Thus, the output waveform of the driving signal is similar the conventional DAC waveform and the difference is that the five lower bits data are modulated by PWM. Thus, the number of current source of different current ratios can be reduced.

FIG. 8 are the waveform of driving signal obtained by the DAC, PWM and present driving method. FIG. 8(a) is the waveform produced by DAC. FIG. 8 (b) is the waveform produced by PWM. FIG. 8(c) is the waveform obtained by the driving method of the present invention, modulated based on the circuit of FIG. 7, using D bit as higher bit. As shown in the drawings, each pulse width of the speaker driving waveform, produced by DAC, are the same; each pulse height of the speaker driving waveform, produced by PWM, are the same; but in accordance with the present invention, the waveform obtained has different height and width.

The driving method of speaker of the present invention divides digital sound data into two groups; one group with bits data being modulated by PWM, the other group with bits data being converted by DAC. Since the number of bits modulated by PWM is reduced, the pulse width level is also reduced. Thus, the frequency of reference clock frequency is relatively low which solves the needs of higher speed clock for PWM. Besides, the number of bits for DAC conversion is also reduced, and the scope of current source variation is narrow which can be controlled within the range of linear variation. Thus, the problems